

DIRECT BROADCAST SATELLITE-RADIO, RECEIVER DEVELOPMENT

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ABSTRACT

This paper reports on the status of the ongoing Direct Broadcast Satellite-Radio (DBS-R) Receiver Development Task being performed at the Jet Propulsion Laboratory, California Institute of Technology (JPL). This work is sponsored by the Voice of America/ U.S. Information Agency through an agreement with NASA.

The objective of this Task is to develop, build, test, and demonstrate a prototype receiver that is compatible with reception of digital audio programs broadcast via satellites. The receiver is being designed to operate under a range of reception conditions, including fixed, portable, and mobile, as well as over a sufficiently wide range of bit rates to accommodate broadcasting systems with different cost/audio quality objectives.

While the requirements on the receiver are complex, the eventual goal of the design effort is to make the design compatible with low cost production as a consumer product. One solution may be a basic low cost core design suitable for a majority of reception conditions, with optional enhancements for reception in especially difficult environments.

Some of the receiver design parameters have been established through analysis, laboratory tests, and a prototype satellite experiment accomplished in late 1991. Many of the necessary design trades will be made during the current simulation effort, while a few of the key design options will be incorporated into the prototype for evaluation during the planned satellite field trials.

BACKGROUND

The DBS-R receiver design effort started as part of a joint NASA/VOA study of digital audio broadcasting via satellite. The motivators for the study were the recognition that the technology for digital audio broadcasting (DAB) via satellite was sufficiently close to maturity to be considered for various domestic and international broadcasting applications, as well as the requirement to help the United States delegation become technically prepared for the 1992 World Administrative Radio Conference (WARC).

The 1992 WARC allocated frequencies for sound Broadcasting Satellite Service (sound), (BSS(sound)) and Complementary Terrestrial Broadcasting in the L-band (1452-1492 MHz), and in two parts of the S-band (2310-2360 MHz) and (2535-2655 MHz). In the United States, satellite sound broadcasting will be implemented in the 2310-2360 MHz band.

The receiver development work will lead to a better definition of satellite sound broadcasting parameters such as signal structure and error protection requirements, margin requirements, and viable service options. The goal of this effort is to stimulate commercialization of satellite sound broadcasting in the U.S. through the transfer of technology to U.S. Industry,

THE PROPAGATION/RECEPTION ENVIRONMENT

Each of the environments that the receiver has to operate in, fixed, portable, and

mobile, influences the signal design or receiver operation in its own unique way. The signal must be designed for operation under the worst conditions, which is usually mobile reception.

The receiver enhancements that can be added to improve performance depend on the reception environment. For mobile reception, enhancements such as the use of channel state information for decoding, and channel equalization will be most useful. For indoor reception, on the other hand, the problems of large values of signal attenuation and frequency selective fading can be eased by enhancements such as more directive antennas and antenna diversity.

Mobile Reception Environment

The mobile propagation environment is characterized by very deep fades caused by blockage of the satellite signal by objects such as trees, buildings and other obstacles. The fades are usually so deep that the signal falls below any practical value of link margin.

Coding and time interleaving are the traditional methods used to combat this effect. The proper choice of coding complexity and interleaving depth are very important. Analysis results show that rate 1/3 rather than rate 1/2 convolutional coding results in better performance under severe blockage conditions, but requires more bandwidth. Longer time interleaving also protects against signal drop out, but requires more memory in the receiver and increases acquisition and re-acquisition times. The use of channel state information in decoding provides transparent performance improvement and is an example of a cost/performance trade that can be made in a mobile receiver.

Indoor Reception Environment

Away from building openings such as windows, the satellite signal suffers significant attenuation, dependent on the type of material

used in the structure. Indoor propagation measurements conducted by the NASA Propagation Program also determined that there can be standing waves with very deep nulls. These nulls can be tens or more MHz wide, so that frequency diversity is not a good solution.

The proposed solutions to indoor reception problems are to use higher gain antennas to overcome the excess building attenuation, and antenna diversity to overcome the standing wave nulls. These are examples of enhancements to the receiver that can be added for indoor reception, but are not needed under other reception conditions.

Design Goals and Solutions

A block diagram of the proposed receiver is shown in Figure 1, with the optional enhancements shown shaded. The receiver consists of a RF portion and a QPSK demodulator. The interface between the two sections is an A to D converter, thus the demodulator will be fully digital.

The functions of the receiver are to receive the satellite signal, demodulate, establish bit and frame synchronization, deinterleave, and decode the convolutionally encoded data.

The receiver will interface with a range of external audio decoders, depending on the type of audio service to be demonstrated. The receiver will support a range of data rates which will, as a minimum, encompass the following:

- AM Quality Digital Audio at 16-32 kbps,
- Monophonic FM Quality Digital Audio at 48-64 kbps,
- Stereo FM Quality Digital Audio at 64-96 kbps,
- Stereo CD Quality Digital Audio at 128-196 kbps.

Even lower data rates or combinations of different data rate programs will be supported by

time multiplexing the separate channels into a single data stream.

It is planned to implement several signal processing options into the prototype receiver for evaluation under field trial conditions, unless they can be eliminated during the simulation phase. These options are:

- Variable interleave length
- Rate 1/2 and 1/3 convolutional coding
- Coherent and pseudo-coherent demodulation

While it is possible to predict to a great extent the performance differences, in terms of bit error rate, of the above options, the impact on audio quality in a complex environment such as mobile reception is not so easy to evaluate under simulated conditions. For this reason these options will remain to be evaluated in the field. Coherent and pseudo-coherent demodulation, since it does not affect signal design, maybe left as selectable options for fixed and mobile reception.

TEST AND EXPERIMENT RESULTS

JPL experience with mobile reception of satellite signals goes back many years with work in the Mobile Satellite area, as well as the 1991 field trials of low rate audio broadcasting with the INMARSAT MARECS B satellite. This work provided a large data base on the propagation characteristics of the mobile channel, which is very useful in simulation and testing of the receiver.

The MARECS B tests used a JPL developed modem operating at 16 kbps and 20 kbps, and a commercial audio codec. One of the goals of the experiment was to evaluate the effects of time interleaving over the range of zero to one second. The effect on bit error rate was as predicted analytically, but was more difficult to assess qualitatively. The problem was that the modem and audio codec operated

independently, and sync loss and reacquisition occurred independently in the two units. Thus overall performance in a difficult reception environment was not as good as it could have been [1],

SIMULATION AND PROTOTYPE IMPLEMENTATION

The receiver is currently being simulated on a Sun workstation, using Comdisco Systems SPW simulation software. Both symbol rate and sample rate simulations are being accomplished. The simulation platform is capable of generating realistic signal characteristics by modeling the signal amplitude and phase on actual field measurements of satellite signals. This is especially important in obtaining a faithful reproduction of the mobile reception environment.

Figure 2 illustrates a simplified block diagram of the DBSR receiver's QPSK demodulator. The simulation algorithm used for determining the performance of the symbol synchronizer and Costas loop is implemented at the symbol rate to avoid excessive simulation time. Therefore, each simulation cycle corresponds to one symbol increment instead of a sample increment. This approach significantly reduces the computation time as compared to simulating the system at the sample rate.

Both analytical and simulation tools are used to obtain the performance of the QPSK demodulator. The outputs of the integrate-and-dump filters are derived analytically, whereas simulation is used for obtaining the outputs of the loop filters, numerically controlled oscillator, update filter, and phase detector. In this figure, the analytical and simulation blocks are denoted by dark-blocks and clear-blocks, respectively. The results of the symbol rate simulation are bit-error-rate, acquisition time and tracking performance, for various receiver parameters [2].

The **DBS-R** digital receiver will be implemented using Field Programmable Gate Arrays (**FPGA**) or Application Specific Integrated Circuits (**ASIC**). This implementation will be accomplished using various Computer Aided Tools. These tools generate a software code representing the digital receiver that can be used for programming a **FPGA** or **ASIC** target chip. This process flow is shown in Figure 3.

From Figure 3, SPW is first used to implement the **DB S-R** receiver using the actual sampling frequency; this is referred to as sample level simulation. At this level, the analytical blocks shown in Figure 2 are implemented using their gate level representation. The sample level simulation is further extended to the hardware level implementation. At this level, the number of binary bits are specified for every component of the receiver; this is referred to as hardware level simulation. The results of the hardware simulation are used for generating the source code for programming the desired target (**FPGA** or **ASIC**). For the prototype receiver, the **FPGA** target was chosen over **ASIC** as the most rapid and economical approach. Therefore, new ideas and design changes can be implemented by simply reprogramming the receiver's **FPGAs**.

PROPOSED SATELLITE EXPERIMENT

After the receiver prototype is built, it is proposed to run a series of field trials with the **TDRS** satellite. This satellite has a 2 degree beam which can be steered around the United States and has enough power and link margin at **S-band** (around 2100 MHz) to support a link up to 256 kilobits. This will allow a comprehensive evaluation of receiver performance under both

outdoor mobile and indoor reception conditions. It will allow a qualitative assessment of the impact of the design options that will still be open.

SUMMARY AND CONCLUSIONS

The **DBS-R** receiver is undergoing the final stages of the design process at **JPL**. Using field measured satellite signal propagation data in the simulation will allow the receiver design to be evaluated under realistic conditions. Digitally compressed audio data will be fed to the receiver mixed with noise and modified by the expected signal impairments. The recovered data will be played back in real time through the audio decompression system for a qualitative assessment of performance with various receiver design options.

While a great part of the design process will be accomplished via simulation, a satellite field trial is planned with a prototype receiver for a final assessment of receiver performance and the completion of any remaining design trades.

REFERENCES

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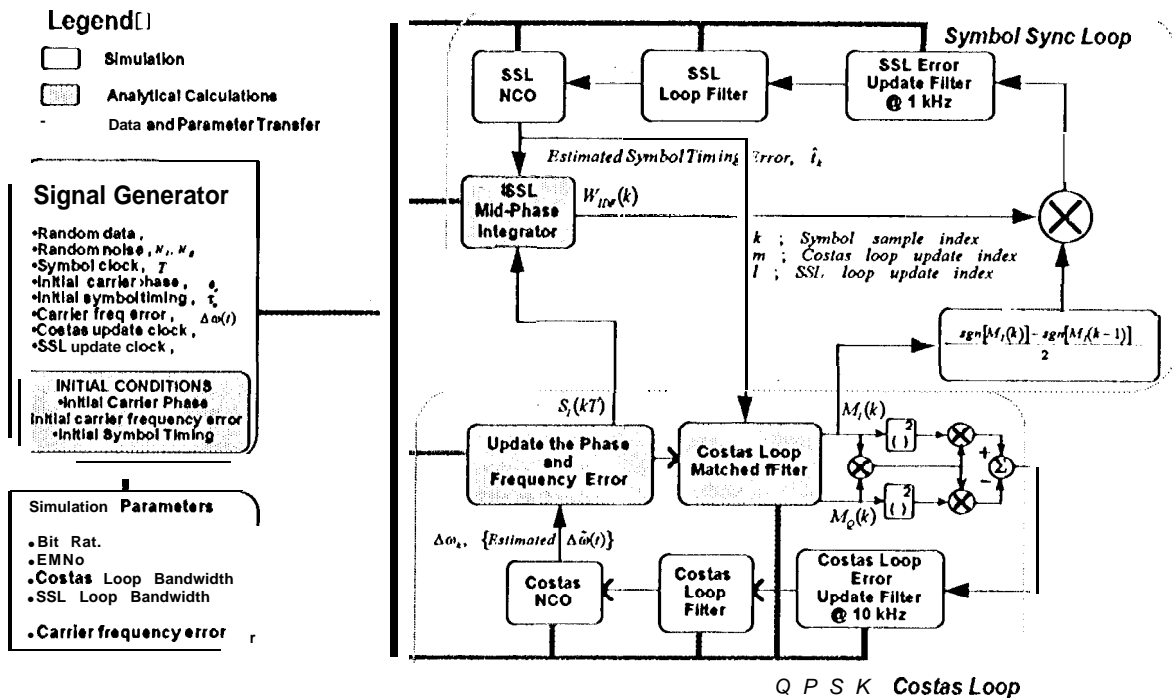
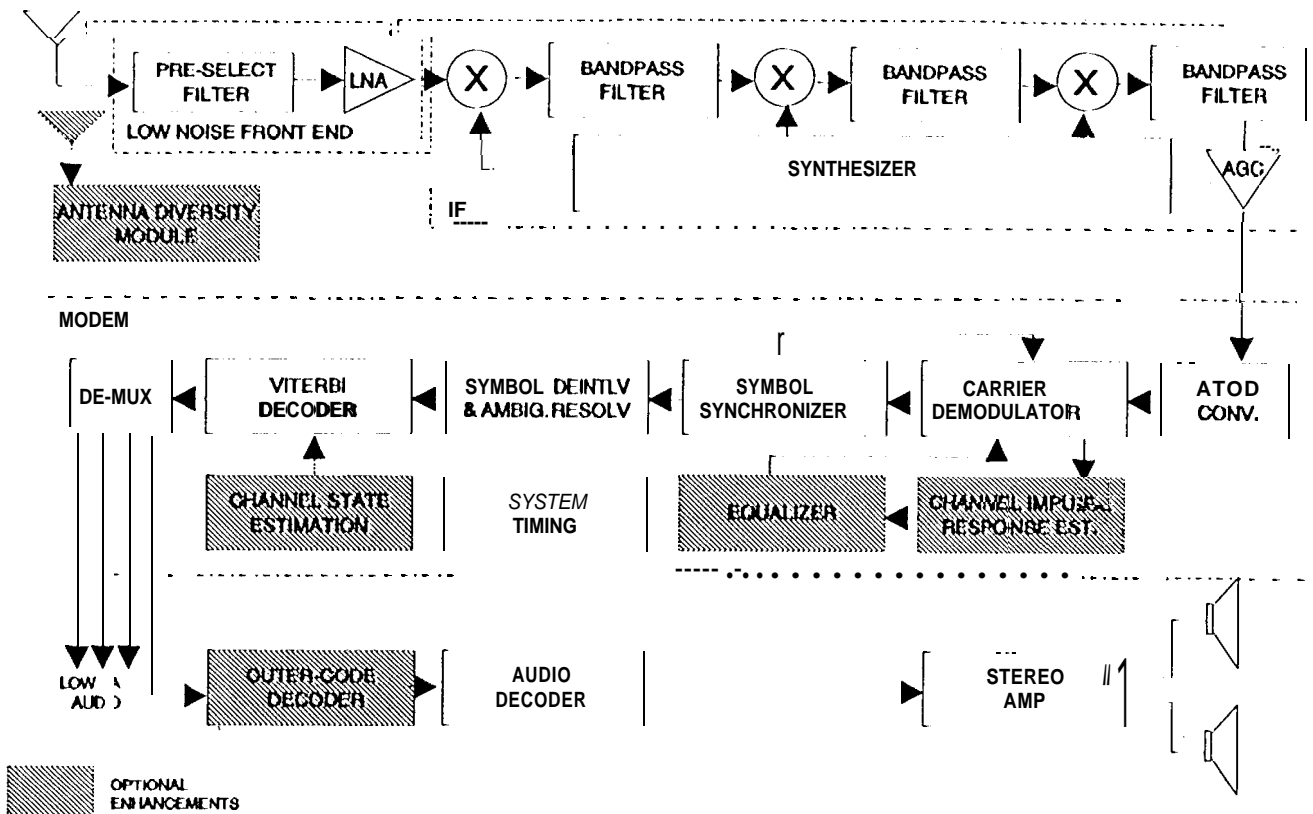


Figure 2. SPW Implementation of the QPSK Demodulator

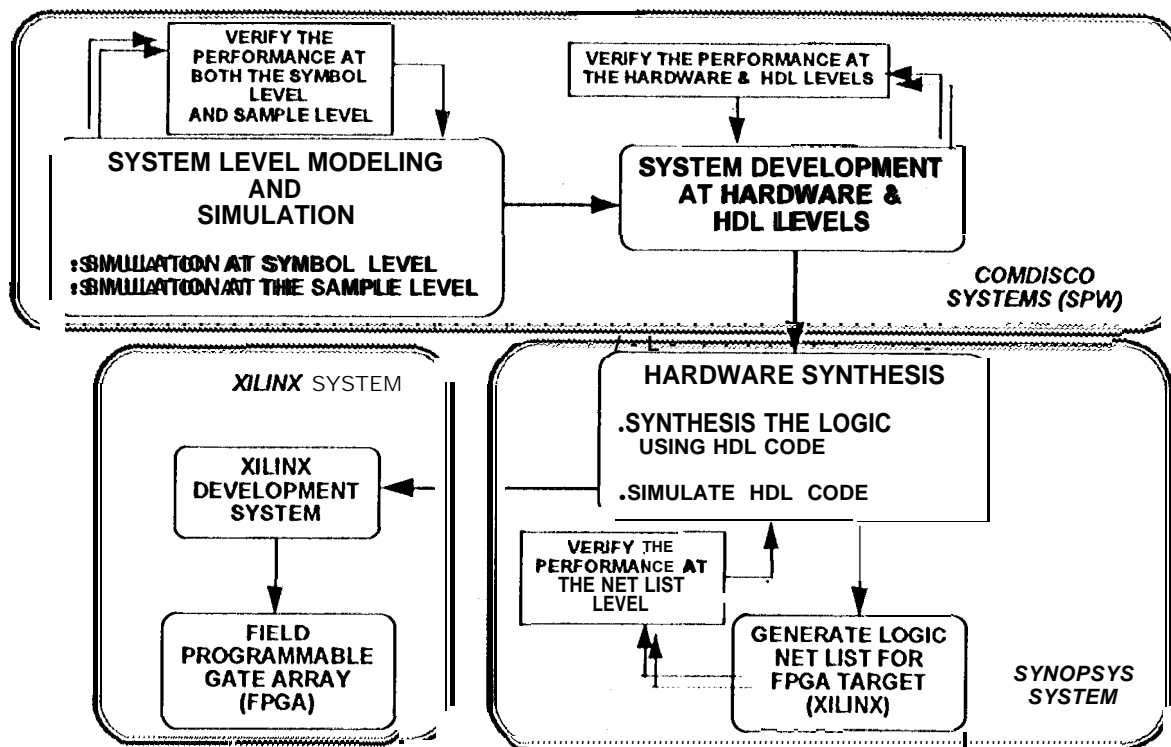


Figure 3. Flow Diagram of Simulation to FPGA implementation